IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: **DeWitt, Jr. et al.**	§	
	§	Confirmation No.: **4157**
Serial No. **10/757,186**	§	
	§	Group Art Unit: **2111**
Filed: **January 14, 2004**	§	
	§	Examiner: **Dang, Khanh**
For: **Method and Apparatus for Qualifying Collection of Performance Monitoring Events by Types of Interrupt When Interrupt Occurs**	§	

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REPLY BRIEF (37 C.F.R. 41.41)

This Reply Brief is submitted in response to the Examiner's Answer mailed on June 9, 2008.

No fees are believed to be required to file a Reply Brief. If any fees are required, I authorize the Commissioner to charge these fees which may be required to IBM Corporation Deposit Account No. 09-0447.

RESPONSE TO EXAMINER'S ANSWER

1) Claims 1-7 are rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter, which Appellants regard as the invention, The Examiner has stated that Appellants' arguments do not relate to the rejection because the hardware counters were not mentioned in the rejection. (See Examiner's Answer, page 16, lines 8-10.) Appellants respectfully disagree. As stated in the Final Office Action and in the Examiner's Answer, claims 1-7 are rejected because "the essential structural cooperative relationships between the so-called "interrupt control mechanism," "interrupt unit," and "performance monitoring unit" have been omitted." (See Examiner's Answer, page 16, lines 11-13.) The portion of the Specification cited by Appellants in the Appeal Brief clearly describes the functional relationship between the performance monitoring unit, which is comprised of the hardware counters, the interrupt unit, and the interrupt control mechanism, which is the interrupt unit control register recited in claim 1. The fact that hardware counters were not recited in the rejection but included in the portion of the Specification cited by the Appellants in the Appeal Brief does not invalidate that the rest of the elements that were rejected were also stated in the cited portion of the Specification and that their functional relationship was clearly described.

On page 14 of the Final Office Action, mailed November 29, 2007, the Examiner suggests that the word "coupled" be provided to overcome the rejection. Appellants respectfully disagree that the term "coupled" is necessary and believe the term to be unnecessarily limiting. The precise layout of components within a processor varies from manufacturer to manufacturer and even within different processors manufactured by the same manufacturer. Therefore, requiring the claim specifically to recite the design of a processor by describing what component is coupled to what component would unnecessarily limit the claims. Further, the actual layout of the components is not crucial to the functioning of the invention. What is required is that the claimed components, the interrupt unit, the interrupt control registers, and the performance monitoring unit, be able to communicate and function as recited in the claims, which is explained in at least the portion of the Specification cited by the Appellants in the Appeal Brief.

2) Claims 1-7 are rejected under 35 U.S.C. § 112, first paragraph, as failing to comply with the written description requirement. Appellants appreciate the Examiner's clarifying the intent of the

rejection. On page 19, lines 24-27, the Specification states "When an interrupt is signaled, the interrupt signal is used to identify whether the counting mechanism of the present invention is programmed to count events during that type of interrupt." Further, page 20, lines 6 through 11 of the Specification states "The IU state mask field indicates the state of interrupt processing during which tracing is to occur. These fields are used by the performance monitoring unit to count events that occur during the various states of the interrupt, and to parse the counting by state." Appellants submit that both of these passages individually support the claimed limitation of "wherein the one or more hardware counters count events that occur during processing of the interrupt responsive to the interrupt unit determining that the interrupt is of the interrupt type selected to be monitored as indicated by the interrupt unit control register."

Additionally, the Specification, on page 21, line 26 through page 22, line 5 states "IUCR such as IUCR1 **308** includes a type field that indicates which interrupt type is to generate a performance monitoring counter signal. The type field in the IUCR is later examined by interrupt unit **304** to see if it is an interrupt type of interest, *i.e.*, whether events are to be counted during execution of the interrupt. If the interrupt type signal is an interrupt type of interest, interrupt unit **304** sends a Tracing On/Off signal to the performance monitoring unit **306** in order to enable or disable counting," which provides explicit detail on how "the one or more hardware counters count events that occur during processing of the interrupt responsive to the interrupt unit determining that the interrupt is of the interrupt type selected to be monitored as indicated by the interrupt unit control register," as recited in claim 1.

Furthermore, page 22, lines 1 through 26 of the Specification states "PMC1 **312** and PMC2 **314** count events that occur during a particular state of interrupt processing. Performance monitoring unit **306** also includes a number of counter control registers (CCRs) such as CCR1 **316** and CCR2 **318**, which may be implemented as MCCR1 **233** and MCCR2 **234** in **Figure 2**. When CCR1 **316** and CCR2 **318** receive signals from interrupt unit **204** to enable or disable tracing events of an interrupt type and state changes during interrupt processing, CCR1 **316** and CCR2 **318** controls counting of the performance monitoring counters PMC1 **312** and PMC2 **314** by storing the current state of the interrupt and the state of the interrupt to trace, so that when tracing is enabled, performance monitoring counters PMC1 **312** and PMC2 **314** may count events of a particular interrupt state. The resulting trace data is then stored and may be collected

at a later time from performance monitoring counters **312** and **314**." This passage of the Specification also support s the feature of "the one or more hardware counters count events that occur during processing of the interrupt responsive to the interrupt unit determining that the interrupt is of the interrupt type selected to be monitored as indicated by the interrupt unit control register," as recited in claim 1.

Page 24, lines 22 through 30 of the Specification states "Preferred embodiments of the present invention can be used to count events based on the type of interrupt during which they occur. Interrupt types are noted in an IUCR field, which indicates the types of interrupt during which monitoring of events is to occur. When an interrupt occurs, the interrupt type is compared to entries in the IUCR, and if the occurring interrupt matches an entry in the IUCR, events that occur during that interrupt are to be counted." Figure 5, and in particular steps **510**-**534**, as described on page 25, line 26 through page 27, line 620, states:

> At some time after the IU trace field is set in step **508**, application code is executed for an application that is to be monitored for performance (step **510**). When an interrupt occurs during code execution (step **512**), the interrupt unit examines the IUCR type field (step **514**). A determination is made as to whether the interrupt is the same type as the IUCR type, which is an interrupt type of interest (step **516**). If the interrupt type is not the same as the IUCR type, the process returns to step **512** to wait for the next interrupt to occur. If the interrupt type is the same as the IUCR type, the interrupt unit raises a Tracing On/Off signal and sends the signal to the performance monitoring unit (step **518**) in order to start tracing events for the interrupt. Once the signal is received, the performance monitoring unit sets the counter control register's state field to interrupt on by setting the bits to 01 (step **520**).
>
> Next, the interrupt state changes to interrupt taken, the interrupt unit in turn raises a state change signal and sends the signal to the performance monitoring unit (step **522**). Consequently, the performance monitoring unit sets the counter control register's state field to interrupt taken by setting the bits to 10 (step **524**). Another interrupt state change causes the interrupt unit to raise a state change signal and sends the signal to the performance monitoring unit (step **526**). Similarly, the performance monitoring unit sets the counter control register's state field to interrupt acknowledged by setting the bits to 11 (step **528**). When the interrupt handler finishes executing the interrupt service routine, it signals the interrupt unit an IRET (interrupt return) (step **530**). The interrupt unit raises a Tracing On/Off signal and sends the signal to the performance monitoring unit in order to stop tracing events for the interrupt (step **532**). (Note that embodiments of the present invention can trace across one or a plurality of states of the interrupt, as described avoce.) Finally, the performance monitoring unit receives the signal and sets the

counter control register state field to interrupt off by setting the bits to 00 (step **534**). Thus, the process terminates thereafter.

Appellants submit that all the above cited passages, whether taken individually or in combination, provides more than adequate support for the recited feature of "the one or more hardware counters count events that occur during processing of the interrupt responsive to the interrupt unit determining that the interrupt is of the interrupt type selected to be monitored as indicated by the interrupt unit control register."

3) Claims 1-6, 8-12, and 16-21are rejected under 35 U.S.C. § 102(b) as being anticipated by *Levine*. In responding to the Examiner's Answer, Appellants had some difficulty in that the portion of the reference cited to by the Examiner did not seem to correspond to what the Examiner was stating. For example, the Examiner quoted the *Levine* reference as stating "MMCR0 is partitioned into a number of bit fields whose settings select events to be counted, enable performance monitor interrupts, specify the conditions under which counting is enabled, and set a threshold value (X)" and cited to *Levine* column 12, lines 4-11 as being the source of the text. However, according to the copy of the reference that Appellants downloaded from the Patent and Trademark Office, the quoted text appears in *Levine*, column 10, lines 60-64. Thus, Appellants had difficulty in ascertaining to what portions of *Levine* the Examiner was actually referring.

As pointed out by the Examiner, *Levine*, in column 10, lines 60-64, states "MMCR0 is partitioned into a number of bit fields whose settings select events to be counted, enable performance monitor interrupts, specify the conditions under which counting is enabled, and set a threshold value (X)." However, Appellants respectfully disagree with the Examiner's conclusion that "**it is clear that bit 5 represents Performance Monitor Interrupt, which is a particular type of interrupt**; and **setting of bit 5 will enable the Performance Monitor Interrupt**." (emphasis in the Examiner's Answer) (see Examiner's Answer, page 20, lines 18-20)

As shown in Figure 6a of *Levine*, bit 5 is merely a bit that enables the generation of an interrupt, the performance monitor interrupt. However, this bit does not indicate the type of interrupt that is to be generated. If one were to merely examine this bit alone, the bit in no way indicates what type of interrupt will be generated by the interrupt unit. Only by knowing that the interrupt unit is part of a performance monitor can one infer the type of interrupt generated by the

interrupt unit, as bit 5 itself does not indicate a type of interrupt. Rather, setting bit 5 merely causes the interrupt unit, of which bit 5 is a part, to generate an interrupt.

Further, claim 1 recites that the interrupt type is of a type selected to be monitored. Responsive to an interrupt being received, a determination is made as to whether the type of the interrupt received is of the interrupt type selected to be monitored. If so, then the hardware counters in the performance monitor count events during processing of the received interrupt. Thus, the interrupt type selected to be monitored, according to claim 1, corresponds to the interrupt that causes counting to occur during the processing of the interrupt.

Levine does not teach such a system. *Levine* does not teach receiving an interrupt and "determining whether the interrupt is of the interrupt type selected to be monitored as indicated by the interrupt unit control register," as recited in claim 1. *Levine* does not teach examining an interrupt to determine what type of interrupt the received interrupt is and comparing this interrupt to an interrupt type selected to be monitored and then "determining whether the interrupt is of the interrupt type selected to be monitored as indicated by the interrupt unit control register."

Further, as stated in *Levine*, column 10, line 54 through column 11, line 20, the MMCR0 counts events, once a threshold value has been exceeded, or has been exceeded a certain number of times, an interrupt is generated. Thus, as taught by *Levine*, the counting of events starts before the generation of an interrupt and only when this counting exceeds a threshold is an interrupt generated. *Levine* does not teach that the interrupt causes counting to occur. In contradistinction, claim 1 recites "count events that occur during processing of the interrupt" and this counting is done "responsive to the interrupt unit determining that the interrupt is of the interrupt type selected to be monitored as indicated by the interrupt unit control register."

The Examiner, on page 21 of the Examiner's answer, alleges that *Levine* teaches that "The Performance Monitor 50 the uses the Performance Monitoring Interrupt to interrupt all activities of the processors, and start performance monitoring." Appellants respectfully disagree. Rather, *Levine* teaches that the performance monitor generates an interrupt once the counting of events has already been started and reached a stage, thus causing the interrupt handler to capture the state of the processor at that time by recording the information in the registers. In contradistinction, claim 1 recites "wherein the one or more hardware counters count events that occur during processing of the interrupt responsive to the interrupt unit determining that the

interrupt is of the interrupt type selected to be monitored as indicated by the interrupt unit control register."

Therefore, for at least the reasons set forth above and in the Appeal Brief filed on April 29, 2008, Appellants respectfully submit that the *Levine* reference does not anticipate claim 1, as the *Levine* reference fails to teach all the features of claim 1.

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